Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A storage device comprising one or more semiconductor memories and an information processing section which performs a first operation for reading data stored in the one or more semiconductor memories and a second operation for writing data to the one or more semiconductor memories in accordance with commands received from outside thereof,

wherein the information processing section detects an error state associated with an area in the semiconductor memory,

substitutes the area during an idle state ~~,~~ ~~where~~in which operations are not being performed in response to the commands, when the error state is ~~indicated~~ detected to be a critical state indicating that the area is usable but in a critical condition requiring substitution, and

substitutes the area immediately when the error state is ~~indicated~~ detected to be a limit state indicating that the area is not usable.

2. (Currently Amended) The storage device according to claim 1,

wherein a factor for the information processing section to determine ~~a~~ the critical state as the error state comprises one or more of an insufficiency of a substitute free area, a successive retry error, a time over of an erasure time or a program time, an erasure count, an over current of performing a read operation or a write operation, and a low current value of externally supplied power; and

wherein a factor for the information processing section to determine ~~a~~ the limit state as the error state comprises one or more of an insufficiency of a substitute free area, a successive retry error, an ECC uncorrectable error at retention failure, a device code unreadable error, a time over of an erasure time or a program time, an erasure count, an over current of performing a read operation or a write operation, and a low current value of externally supplied power.

3. (Currently Amended) The storage device according to claim 2, and which is capable of independently setting the factors for the information processing section, to determine ~~a~~ the critical state and setting the factors

for the information processing section to determine ~~a~~ the limit state.

4. (Original) The storage device according to claim 3,

wherein a substitution destination area substituted by the information processing section is a free area in the semiconductor memory or semiconductor memory for substitution only.

5. (Original) The storage device according to claim 4,

wherein, when the substitution destination area is a free area in the semiconductor memory, the substitution destination area is a physical area controlled by an individual peripheral circuit which controls any of a plurality of sectors provided for a memory mat.

6. (Currently Amended) The storage device according to claim 5, wherein a decode method of the device substitutes only data in a substitution origin area for data in ~~a~~ the substitution destination area, and after substitution, allows access to the substitution destination area instead of the substituted area, and allows access to

an unsubstituted area in the same manner as before the substitution.

7. (Previously Presented) The storage device according to claim 1,

wherein the information processing section notifies an outside of an emergency condition when the error state is indicated to be the limit state.

8. (Previously Presented) The storage device according to claim 7, wherein one or more restricting operations, including inhibiting a write operation, are performed in the limit state.

9. (Currently Amended) The storage device according to claim 8,

wherein the information processing section copies data from ~~a~~ the substitution origin area to ~~a~~ the substitution destination area during the area substitution and corrects a correctable error if it is contained in the data.

10. (Currently Amended) The storage device according to claim 9, further comprising:

a detection circuit for detecting an area state;

a notification circuit for notifying ~~an~~ the outside of a detection result and an area substitution state;

an area substitution circuit for performing area substitution; and

an area decode management circuit for managing permission or inhibition of access to areas.